UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/590,621	06/08/2000	Salman Akram	3936US (99-0066)	1302

7590 10/25/2004

Brick G Power
Trask Britt & Rossa
P O Box 2550
Salt Lake City, UT 84110

EXAMINER	
BEREZNY, NEMA O	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 10/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/590,621	AKRAM	
	Examiner	Art Unit	
	Nema O Berezny	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24 and 27-36* is/are rejected.

7)☒ Claim(s) *25 and 26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 June 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12152003,05132004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after allowance or after an Office action under *Ex Parte Quayle*, 25 USPQ 74, 453 O.G. 213 (Comm'r Pat. 1935). Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on 12-15-03 has been entered.

Claims 1-36 are currently pending.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-6, 8-23, 36-37, and 40-49 are rejected under 35 U.S.C. 102(e) as being anticipated by Griff (6,740,962). The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference,

it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Griff discloses a method of modifying a semiconductor die, comprising: providing at least one semiconductor die (Fig.8A el.32) having an active surface (el.33); and forming on or securing to said active surface at least one stabilizer (el.20) comprising at least two superimposed, contiguous, mutually adhered lavers comprising a dielectric material (col.4 lines 45-53; col.6 lines 11-20) such that said at least one stabilizer protrudes from said active surface, said at least one stabilizer being configured to space said at least one semiconductor die a substantially fixed distance apart from a higher-level substrate (el.40) when disposed active surface-down over said higher-level substrate (Fig.8A) **[claim 1]**. Griff also discloses wherein said forming said at least one stabilizer comprises forming a plurality of stabilizers (Figs.4, 8A) **[claim 2]**; wherein said forming said plurality of stabilizers comprises forming at least one stabilizer of said plurality of stabilizers adjacent at least one corner of said active surface (Fig.8A) **[claim 3]**; wherein said forming said plurality of stabilizers comprises forming at least two stabilizers adjacent opposite peripheral edges of said active surface (Fig.8A) **[claim 4]**; wherein said forming said plurality of stabilizers comprises forming selected ones of said plurality of stabilizers to have a height that defines a substantially consistent die-to-substrate distance (Fig.8A) **[claim 5]**; wherein said forming said at least one stabilizer

comprises forming said at least one stabilizer from photoimageable material (col.4 lines 24-26; col.6 lines 13-16) **[claim 6]**; wherein said providing comprises providing at least one semiconductor die having a sealing material (el.14) on an active surface thereof and wherein said forming comprises forming said at least one stabilizer to be securable to said sealing material (col.6 line 11) **[claim 7]**; wherein said providing comprises providing a semiconductor wafer including a plurality of semiconductor dice (col.15 lines 28-30) **[claim 8]**; adhering (el.14) said at least one stabilizer to said active surface (Fig.8A; col.7 line 66 – col.8 line 11) **[claim 9]**; wherein said forming said at least one stabilizer comprises applying a layer of insulative material on said active surface and patterning said layer (col.8 line 55 – col.9 line 5) **[claim 10]**; wherein said forming said at least one stabilizer comprises applying a layer of photoresist material on said active surface and patterning said layer (col.9 lines 6-13) **[claim 11]**; introducing an encapsulant material between said at least one semiconductor die and said substrate (col.7 lines 36-40) **[claim 12]**; wherein said forming said at least one stabilizer comprises positioning said at least one stabilizer on said active surface so as to avoid contact with conductive traces on a carrier substrate (col.7 lines 30-35) **[claim 13]**; disposing at least one conductive structure (el.28) on at least one bond pad (el.16b) of said at least one semiconductor die **[claim 14]**; wherein said disposing comprises forming a solder bump on said at least one bond pad (Fig.8A) **[claim 15]**; and wherein said disposing comprises applying one of a conductive pillar (el.28), a conductor filled epoxy pillar, and a structure of z-axis elastomer to said at least one bond pad (Fig.8A) **[claim 16]**.

Grigg also discloses a method of modifying a semiconductor device component, comprising: providing at least one semiconductor substrate (Fig.8A el.32) with contact pads (el.16b) on an active surface (el.33) thereof; and sequentially forming on said active surface at least one stabilizer (el.20) having a plurality of superimposed, contiguous, mutually adhered layers of photopolymer (col.4 lines 23-25, 45-53; col.6 lines 11-20), said at least one stabilizer being configured to at least partially stabilize an orientation of the semiconductor device component upon being disposed active surface-down over a higher-level substrate (Fig.8A el.40; col.6 lines 58-61; col.9 lines 22-26; col.10 lines 31-51) **[claim 17]**. Grigg also discloses a method of modifying a semiconductor device component, comprising: placing at least one semiconductor substrate (Fig.8A el.32) having an active surface (el.33) with contact pads (el.16b) exposed thereon in a horizontal plane (Fig.8A); recognizing a location and orientation of said at least one substrate (col.4 lines 54-61; col.13 lines 4-6; col.15 lines 9-13); stereolithographically forming on said active surface, between one of said contact pads and a peripheral edge of said at least one substrate (Fig.5) , at least one stabilizer (el.20) comprising at least one layer of an electrically nonconductive semisolid material (col.4 lines 45-53; col.6 lines 11-20; col.9 lines 47-53; col.10 lines 31-51) **[claim 18]**. Grigg also discloses further comprising storing data including at least one physical parameter of said at least one substrate in computer memory, and using the stored data in conjunction with a machine vision system to recognize said location and orientation of said at least one substrate and to form said at least one stabilizer thereon (col.12 lines 51-63) **[claim 19]**; further including in computer memory at least one parameter of

another semiconductor device component to which said at least one substrate is to be attached (col.12 lines 51-63) **[claim 20]**; further comprising using stored data, in conjunction with said machine vision system, to selectively form said at least one layer of semisolid material stereolithographically on at least one portion of said active surface of said at least one substrate (col.12 lines 51-63; col.12 lines 51-63) **[claim 21]**; and further including securing said at least one substrate to a carrier prior to placing said at least one substrate in said horizontal plane (col.9 lines 22-26) **[claim 22]**.

Grigg also discloses a method for electrically bonding a semiconductor device component having a surface and conductive structures protruding from said surface to a substrate having contacts positioned correspondingly to said conductive structures, said method comprising: stereolithographically forming at least one stabilizer structure comprising a dielectric material on at least one of said surface and said substrate for disposal between said surface and said substrate (col.4 lines 45-53; col.6 lines 11-20; col.9 lines 47-53; col.10 lines 31-51); inverting and positioning said semiconductor device component on said substrate to contact said conductive structures to corresponding contacts (Fig.8A); and bonding said conductive structures to the corresponding contacts (Fig.8A) **[claim 23]**. Grigg also discloses wherein said stereolithographically forming at least one stabilizer structure comprises forming said at least one stabilizer structure to have a height less than a minimum distance said conductive structures protrude from said surface (Fig.8A) **[claim 24]**; and wherein said stereolithographically forming at least one stabilizer structure comprises configuring said at least one stabilizer structure to be positioned between a periphery of said surface of

said semiconductor device component and said conductive structures (Fig.5) **[claim 27]**.

Grigg also discloses a method of modifying a semiconductor die, comprising: providing at least one semiconductor die (Fig.8A el.32) having an active surface (el.33) with contact pads (el.16b) exposed thereon; applying a layer of a partially uncured photopolymer to said semiconductor; and stereolithographically forming on said semiconductor, between one of said contact pads and a peripheral edge of said semiconductor, at least one stabilizer securable to said active surface so as to protrude from said active surface, said at least one stabilizer being a structure configured to at least partially stabilize an orientation of said at least one semiconductor die when disposed active surface-down over a higher-level substrate (col.4 lines 45-53; col.6 lines 11-20; col.9 lines 47-53; col.10 lines 31-51) **[claim 28]**. Grigg also discloses wherein said forming said at least one stabilizer comprises forming a plurality of stabilizers (Figs.4, 8A) **[claim 29]**; wherein said forming said plurality of stabilizers comprises forming at least one stabilizer of said plurality of stabilizers adjacent at least one corner of said active surface (Fig.8A) **[claim 30]**; wherein said forming said plurality of stabilizers comprises forming selected ones of said plurality of stabilizers to have a height that defines a substantially consistent die-to-substrate distance (Fig.8A) **[claim 31]**; wherein said providing comprises providing a semiconductor wafer including a plurality of semiconductor dice (col.15 lines 28-30) **[claim 32]**; further comprising introducing an encapsulant material between said at least one semiconductor die and said substrate (col.7 lines 36-40) **[claim 33]**; wherein said forming said at least one

stabilizer comprises positioning said at least one stabilizer on said active surface so as to avoid contact with conductive traces on a carrier substrate (col.7 lines 30-35) **[claim 34]**; further comprising disposing at least one conductive structure (el.28) on at least one bond pad (el.16b) of said at least one semiconductor die **[claim 35]**; and wherein said disposing comprises forming a solder bump (el.28) on said at least one bond pad (Fig.8A) **[claim 36]**.

Allowable Subject Matter

The following is a statement of reasons for the indication of allowable subject matter for claims 25-26: the prior art of record does not teach or disclose a method for electrically bonding a semiconductor device component having a surface and conductive structures protruding from said surface to a substrate having contacts positioned correspondingly to said conductive structures, said method comprising inter alia: wherein said stereolithographically forming at least one stabilizer structure comprises forming said at least one stabilizer structure to space said surface from said substrate a distance greater than a minimum distance at least one of said conductive structures protrudes from said surface; and wherein said bonding comprises employing said at least one stabilizer structure to lengthen at least one of said conductive structures. Grigg does not specifically disclose said features. Since the assignee of said instant specification and the Grigg (6,740,962) patent are the same and the Grigg patent only qualifies as a 102(e) prior art reference, no other reference can be combined with Grigg to make a 103(a) rejection.

Claims 25-26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nema O Berezny whose telephone number is (571) 272-1686. The examiner can normally be reached on M-F 9-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NB

Nema Berezny